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miss and (queue or buffer) and address and

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#### [Store queue for a tightly coupled multiple processor configuration with two-level cache buffer ...](#)

SL Gregor - US Patent 5,023,776, 1991 - [freepatentsonline.com](#)

... if the search resulted in an L2 cache directory miss. ... write buffers and L2 store queues are all ... The aforementioned L2 write buffer controls (L2WB CTLS) are ...

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#### [Cache miss buffer adapted to satisfy read requests to portions of a cache fill in progress without ...](#)

RN Patel, A Malami, NM Hayes... - US Patent 5,353,426, 1994 - [freepatentsonline.com](#)

... causes read signals and the physical address to be ... indicator in the instruction/data cache miss buffer, block 96 ... to be provided to the instruction queue, one of ...

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#### [Virtual address table look aside buffer miss recovery method and apparatus](#)

RP Colwell, JO'Donnell, DB Papworth, PK Rodman - US Patent 4,920,477, 1990 - [freepatentsonline.com](#)

... illustrating the elements of the status queue data word in ... provides an indication of the cache miss read state ... PC data through a bidirectional buffer 299b over ...

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#### [History-based prefetch cache including a time queue](#)

AD Berenbaum, TE Jeremiassen... - US Patent 5,778,435, 1998 - [freepatentsonline.com](#)

... e) correlating an address of a cache miss with an event in the time queue and inserting the cache miss address into the prefetch target buffer indexed and ...

[Cited by 18](#) - [Related articles](#) - [Web Search](#) - [All 3 versions](#)

#### [\[PDF\] ► The Alpha 21264 Microprocessor: Out-of-Order Execution at 600 MHz](#)

RE Kessler, MA Shrewsbury - IEEE, editor, Hot chips - [courses.ece.uiuc.edu](#)

... Int Issue Queue (20) Exec 4 Instructions / cycle ... 128-bit 44-bit Victim Buffer L1 Data Cache ... Addr Miss Address Branch Predictors Next-Line Address L1 Ins. Cache ...

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#### [Improving direct-mapped cache performance by the addition of a small fully-associative cache and ...](#) - ► [kookmin.ac.kr](#) [PDF]

NP Jouppi - Computer Architecture, 1990. Proceedings. 17th Annual ..., 1990 - [ieeexplore.ieee.org](#)

... caching, refetch cache lines starting at a cache miss address. \$he prefetched data is placed in the buffer and not in the cache. ...

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#### [Exploiting Choice: Instruction Fetch and Issue on an Implementable Simultaneous Multithreading ...](#) - ► [uiuc.edu](#) [PDF]

HM Levy, JL Lo, JS Emer, RL Stamm, SJ Eggers, DM ... - [ieeexplore.ieee.org](#)

... provided by a decoupled branch target buffer (BTB) and ... thousand instructions 3 5 9 L3 cache miss rate 55.1 ... cycles) 14% 9% 3% avg (combined) queue population 25 ...

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#### [UltraSPARC-III: designing third-generation 64-bit performance](#)

T Horel, G Lauterbach, SM Inc, P Alto - Micro, IEEE, 1999 - [ieeexplore.ieee.org](#)

... path buffering in the I stage (the miss queue). ... of instructions; enqueue instructions into the queue J Steer ... and instruction address translation buffer access. ...

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#### [Power and performance tradeoffs using various caching strategies](#) - ► [virginia.edu](#) [PDF]

RI Bahar, G Albera, S Manne - Low Power Electronics and Design, 1998. Proceedings, 1998 ..., 1998 - [ieeexplore.ieee.org](#)

... associated with each first level cache; this buffer was implemented as ... Load/Store Queue Entries 16 Fetch Queue 16 Minimum ... 011 a miss, we use a write-back, write ...

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#### [Methods and apparatus for improving cache consistency using a single copy of a cache tag memory in ...](#)

JH Chang, C Berg, J Cruz-Rios... - US Patent 5,398,325, 1995 - [freepatentsonline.com](#)

... write, write-invalidate, and write-miss operations associated ... block to be written to the invalidation queue. ... also written to the output buffer holding pending ...

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Key authors: [N Jouppi](#) - [H Levy](#) - [R Kessler](#) - [J Lo](#) - [J Emer](#)

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miss and (queue or buffer) and add

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